UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/780,208	02/09/2001	Hungyu H. Hou	M-9662 US	6979

7590 11/19/2003

Philip W. Woo
c/o Sidley Austin Brown & Wood LLP
555 California Street
Suite 5000
San Francisco, CA 94104-1715

EXAMINER
PATEL, PARESH H

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/780,208	HOU ET AL.	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35 and 37-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *11* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Fax document (3 pages)* .

DETAILED ACTION

1. Claim 34 is withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant elects species 1 (claims 1-33, 35 and 37-48) with traverse Paper No. 9. **However, Examiner will examine claim 34 in order to expedite the prosecution because it do not distinguish over prior art. In future if restriction is proper, it may be set forth.**

Response to Arguments

2. Applicant's arguments filed 09/19/2002 have been fully considered but they are not persuasive.

3. On page 13, first paragraph applicant argues, "None of the features identified by the Examiner as a ***selectable threshold point circuit*** *i. e. "[fig. 5 or 7 or 8 or 10]"* of Yakin are a ***selectable threshold point circuit***." Examiner disagrees because the selectable threshold point circuit as defined in office action is used to select one of the pluralities of values for a threshold point of the power supply [see lines 28-47 of column 6 where Yakin discloses that "a threshold voltage is controllable by appropriate selection of these control voltages" i. e. Vc1 through Vc4].

4. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in

the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Furuno discloses semiconductor IC which is operable and programmable (selectable) at multiple voltage levels [see Vcv of fig. 2 with fig. 7] and Yakin discloses selectable threshold voltage circuit (using control signals Vc1 through Vc4) which outputs adjustable logic signal depends upon selected threshold voltage, hence combination of Yakin and Furuno will provide programmable (selectable) output at constant voltage.

5. On page 14 applicants argues, "neither Yakin nor Furuno, separately or in combination, teaches, discloses or suggests a selectable threshold point circuit connected to a voltage following circuit." Examiner again disagrees because office action of paper no 4 wherein Yakin at lines 9-18 of column 2 (specifically "adding circuitry for ... reducing power supply drift") discloses this limitation.

6. Examiner agrees with applicant's arguments on page 15, particularly for claim 21, about Furuno's "A system". It should read Fig. 13 instead fig. 1.

7. On page 16, applicant argues, "claim 16 contains limitation as to selecting, tracking and generating not shown to be found in the prior art". Examiner disagrees because: selecting one of a plurality of values for a threshold point is discloses by Yakin [see last three lines of abstract]; tracking the voltage value of the power supply is also disclosed by Yakin [see first four lines of abstract]; and generating the output is also disclosed by Yakin [see V_L].

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 37-42 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claim 37, disclosure does not support "a first sense" and "a sense opposite to the first sense" as claimed.

All dependent claims are rejected because they depend from rejected claim.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 37-48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 37, "a selectable threshold point circuit operable to conduct a reference current ... in a first sense; and a switch circuit operable ... in a sense opposite to the first sense," where in **a first sense** and **a sense opposite to the first sense** is not clear and have following concern/question(s): 1) what is a first sense of a control

signal? 2) what is a first sense of supply voltage? 3) what is a first sense of a threshold voltage? With respect to other limitation "a sense opposite to the first sense" Examiner have same question(s) and concern(s) as mention earlier, in short it is unclear what is an opposite sense. Also it is not clear how selected one of the plurality of predefined current magnitudes **limits** the voltage-controlled current.

Regarding claim 43, what is not clear is "generating an output … by determining whether the selected amount of current acts to **limit** a further current".

Regarding claim 48, what is not clear is relation between "a first state of the output signal," "a first condition" and "the further transistor acts to **limit** a sum of the reference current magnitudes". Similarly relation between "a second state of the output signal," "a second condition" and "the selectable threshold point circuit acts to **limit** the switch current magnitudes" is not clear from the disclosure.

All dependent claims are also rejected because they depend from rejected claim(s).

10. For the purpose of Examination and in order to expedite the prosecution examiner assumes that ***a first sense*** *means when supply voltage is less than threshold voltage and a selectable threshold point to circuit is operable.* ***A sense opposite to the first sense*** *means when supply voltage is greater than threshold voltage and a switch circuit is operable.*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuno et al. (US 5444663) in view of Yaklin (US 6157222).

Regarding claim 1 Furuno et al. (hereafter Furuno) discloses : A voltage detector [fig. 2] comprising:

a voltage following circuit [fig. 4 or 6] connected to a power supply [Vref of fig. 2] and operable to follow a voltage value of the power supply; and

a switch circuit [fig. 5] coupled to the selectable threshold point circuit [fig. 7] and the voltage following circuit; the switch circuit cooperating with the selectable threshold point circuit to generate an output indicating whether the value of the power supply has increased above or decreased below the selected value for the threshold point in response to the followed value of the power supply.

Furuno discloses all the elements of the claimed invention except for a selectable threshold point circuit connected to the voltage following circuit and operable to select one of a plurality of values for a threshold point of the power supply. Rather, Furuno discloses a supply voltage decision circuit [fig. 7] which outputs a signal corresponding to the input supply voltage. Yakin discloses a selectable threshold point circuit [fig. 5 or 7 or 8 or 10] connected to the voltage following circuit [lines 9-18 of column 2] and

operable to select one of a plurality of values for a threshold point of the power supply [fig. 9]. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide voltage detector of Furuno with the selectable threshold point circuit of Yaklin in order to provide a constant voltage to an internal circuit of IC during testing/normal operation.

Regarding claims 2 and 22, Yaklin discloses: the selectable threshold point circuit is operable to receive a plurality of control signals [element VC1, VC2, VC3 of fig. 5].

Regarding claims 3 and 23, Yaklin discloses: the selectable threshold point circuit is operable to output a programmable amount of current [fig. 5 and 6].

Regarding claims 4 and 24, Yaklin discloses: the selectable threshold point circuit comprises a plurality of current mirror transistors [element T21/T20 and T23/T22 of fig. 10].

Regarding claims 5 and 25, Yaklin discloses: at least one of the current mirror transistors is coupled to a respective switch transistor [element T15 and T16 of fig. 10].

Regarding claims 6 and 26, Yaklin discloses: the switch transistor is operable to receive a control signal [element V_{CAL} of fig.10].

Regarding claims 7 and 27, Yaklin discloses: the selectable threshold point circuit comprises a plurality of current mirror transistors, at least two of the current mirror transistors having a different width-to-length ratio [lines 30-34, 54-58 and 62-65 column 4].

Regarding claims 8 and 28, Furuno discloses: the switch circuit comprises a transistor [elements Q1 or Q2 of fig. 5].

Regarding claims 9 and 29, Furuno discloses: a gate of the transistor [element Q1 of fig. 5] receives the followed value of the power supply [element N1 of fig. 5].

Regarding claims 10 and 30, Yaklin discloses: the switch circuit and the selectable threshold point circuit are connected at a detection node, the switch circuit operable to pull a voltage at the detection node to ground when the value of the power supply is above the selected value for the threshold point [lines 20-22 of column 5 and lines 30-34 of column 6].

Regarding claims 11 and 31, Yaklin discloses: the switch circuit and the selectable threshold point circuit are connected at a detection node, the selectable threshold point circuit operable to pull a voltage at the detection node up to the value of the power supply when the power supply is below the selected value for the threshold point [lines 22-25 of column 5 and lines 35-38 of column 6]. .

Regarding claims 12 and 32, Furuno discloses: a current source generator block [fig. 3and 2] coupled to the voltage-following circuit and the switch circuit.

Regarding claims 13 and 33, Furuno discloses: the current source generator block comprises: a reference transistor [element Q1 of fig. 3]; and a current mirror transistor [element Q4 and Q5 of fig. 3] coupled to the reference transistor and the switch circuit.

Regarding claims 14 and 34, Furuno discloses: the current source generator block comprises: a reference transistor [element Q14 of fig. 3]; and a plurality of current

mirror transistors [element Q4/Q5 and Q11/Q12 of fig. 3] coupled to the reference transistor and the switch circuit.

Regarding claims 15 and 35, Furuno discloses: a voltage level detection circuit [fig. 7] coupled to the selectable threshold point circuit and the switch circuit, the voltage level detection circuit operable to output a signal [element V_{CH} of fig. 2] whether the value of the power supply is above or below the selected value for the threshold point.

Regarding claims 16-20, clearly the above discussed combination of Furuno in view of Yaklin will provide the recited method.

Regarding claim 21, Furuno discloses: A system [fig. 13] comprising:

a memory [see fig. 13];

a microprocessor [see fig. 13] ; and

a voltage detector [fig. 2] coupled to the memory and the microprocessor, the voltage detector comprising:

a voltage following circuit [fig. 4 or 6] connected to a power supply [Vref of fig. 2] and operable to follow a voltage value of the power supply; and

a switch circuit [fig. 5] coupled to the selectable threshold point circuit [fig. 7] and the voltage following circuit; the switch circuit cooperating with the selectable threshold point circuit to generate an output indicating whether the value of the power supply has increased above or decreased below the selected value for the threshold point in response to the followed value of the power supply.

Furuno discloses all the essential elements of the claimed invention except for a selectable threshold point circuit connected to the voltage following circuit and operable

to select one of a plurality of values for a threshold point of the power supply. Yakin discloses a selectable threshold point circuit [fig. 5 or 7 or 8 or 10] connected to the voltage following circuit [lines 9-18 of column 2] and operable to select one of a plurality of values for a threshold point of the power supply [fig. 9]. Rather, Furuno discloses a supply voltage decision circuit [fig. 7] which outputs a signal corresponding to the input supply voltage. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide system of Furuno with the selectable threshold point circuit of Yaklin in order to provide a constant voltage to an internal circuit of IC during testing/normal operation.

12. Claims 37 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuzumoto (US 5132565).

Regarding claim 37, Kuzumoto discloses: A voltage detector [fig. 1] energized by a supply voltage [Vex] and comprising:

a selectable threshold point circuit [1] operable to conduct a reference current having a selected one of a plurality of predefined current magnitudes through a circuit node [output node of 4] in a first sense [see abstract when Vex does not exceed the threshold voltage]; and

a switch circuit [2] operable to conduct a voltage-controlled current through the circuit node [node at the output of 4] in a sense opposite to the first sense [see abstract when Vex exceed the threshold voltage], a magnitude of the voltage controlled current being responsive to a magnitude of the supply voltage [inherent to 2], the switch circuit further operable to generate an output indicating whether the supply voltage exceeds a

threshold value [see abstract] responsive to whether the selected one of the plurality of predefined. current magnitudes limits the voltage-controlled current.

Kuzumoto discloses all the elements except for the switch circuit further operable to generate an output indicating whether the supply voltage exceeds a threshold value **responsive to whether the selected one of the plurality of predefined current magnitudes limits the voltage-controlled current.** It would have been an obvious matter of design choice to modify Kuzumoto's switch circuit, since applicant has not disclosed that output of switch circuit responsive to whether the selected one of the plurality of predefined current magnitudes limits the voltage-controlled current solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well.

Regarding claim 43, clearly the above discussed Kuzumoto reference will provide the recited method.

13. Claims 38-42 and 44-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuzumoto as applied to claims 37 and 43 above, and further in view of Yaklin (US 6157222).

Regarding claim 38 Kuzumoto discloses all the elements except for the voltage detector of Claim 37 wherein**: the selected one of a plurality of predefined current magnitudes is selected in response to a plurality of control signals**. Yakin discloses a selectable threshold point circuit [fig. 5 or 7 or 8 or 10] connected to the voltage following circuit [lines 9-18 of column 2] and **operable to select one of a plurality of predefined current magnitudes is selected in response to a plurality of**

control signals [fig. 9 and using element VC1, VC2, VC3 of fig. 5]. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide detector of Kuzumoto with the selectable threshold point circuit operable to select one of predefined current magnitude of Yaklin in order to provide a constant desire voltage to an internal circuit of IC during testing and/or normal operation.

Regarding claim 39, Yaklin discloses: the selectable threshold point circuit comprises a plurality of current mirror transistors [element T21/T20 and T23/T22 of fig. 10].

Regarding claim 40, Kuzumoto discloses: the switch transistor is operable to receive a control signal [input to PT_9 and/or PT_{10} of 2 and/or PT_{18}].

Regarding claim 41, Yaklin discloses: the selectable threshold point circuit comprises a plurality of current mirror transistors, at least two of the current mirror transistors having a different width-to-length ratio [lines 30-34, 54-58 and 62-65 column 4].

Regarding claim 42, Kuzumoto discloses: the switch circuit comprises a transistor [PT_9 and/or PT_{10} and/or PT_{18}].

Regarding claims 44-47, clearly the above discussed combination of Kuzumoto in view of Yaklin will provide the recited method.

14. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujitsu Semiconductor Data Sheet (Fujitsu MB3771 Power supply monitor) in view of Yakin.

Regarding claim 48, Fujitsu Semiconductor Data Sheet (hereafter Fujitsu) discloses: A voltage detector [Fujitsu MB3771] energized by a supply voltage [see power supply of page 1 and Vcc], the detector comprising:

a plurality of control signal terminals [see PIN ASSIGNMENT on page 2 and terminal 1-2, 6-8] of receiving a plurality of control signals [signals as shown at pins 1-2, 6-8 on page 2];

a selectable threshold point circuit [Reference Voltage, comparator A, B, OR Gate, AND Gate, FF, Transistor connected to FF, comparator connected to OR Gated and a comparator connected to transistor of pin 8 of page 3];

a further transistor [transistor connected to terminal 8 of page 3] and further having a control terminal [base terminal] controlled by the supply voltage, the further transistor operable to conduct a switch current having a switch current magnitude [10 micro amp source of page 3] responsive to a magnitude of the supply voltage [Vcc];

an output terminal [terminal RESET (8) of page 3] carrying an output signal responsive to a voltage at the common circuit node [node where terminal 1 and 8 is connected], a first state of the output signal corresponding to a first condition [lines 1-4 under Functional Explanation of page 3] wherein the further transistor acts to limit a sum of the reference current magnitudes, and a second state of the output signal corresponding to a second condition [lines 1-4 under Functional Explanation of page 3] wherein the selectable threshold point circuit acts to limit the switch current magnitude, whereby the voltage detector detects a sufficiency of the supply voltage [lines 6-11 of page 3];

a plurality of control signal terminals [see PIN ASSIGNMENT on page 2 and terminal 1-2, 6-8] of receiving a plurality of control signals [signals as shown at pins 1-2, 6-8 on page 2];

a common circuit node [node between 12 micro amp. Source and a transistor of page 3].

Fujitsu discloses all the elements except for a selectable threshold point circuit comprising **a plurality of transistors** connected to a common node, each transistor of the plurality of transistors operable to conduct a respective reference current magnitude and to be controlled by a respective control signals. However, Fujitsu is silent about use of plurality of transistor and electrical connection, but discloses generation of different voltage/current using component shown in fig. Of page 3]. Yakin discloses a selectable threshold point circuit [fig. 5] comprising **a plurality of transistors** [T2-T9] connected to a common node [V_{OUT}], each transistor of the plurality of transistors operable to conduct a respective reference current magnitude and to be controlled by a respective control signals [V_{IN}, VC1-VCN]. It would have been obvious to use or modify Fujitsu with plurality of transistor and control signals as taught by Yakin, in order to achieve precision and adjustability requirement for setting a threshold level by reducing circuit complexity and power consumption.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 703-306-5859. The examiner can normally be reached on 8:00 to 4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 703-308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Paresh Patel
October 31, 2003

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800